REMARKS

This application has been reviewed in light of the Office Action dated April 14, 2005. Claims 1-4 and 6-12 are pending in this application. Claims 1-4 and 8-11, the independent claims, have been amended to define still more clearly what Applicant regards as his invention. Favorable reconsideration is requested.

Claims 1-4 and 6-12 were rejected under 35 U.S.C. § 103(a) as being obvious from European Patent Application 0905978 A2 to Yip et al. ("Yip EU") in view of Australian Patent Publication 199957151 A1 to Yip et al. ("Yip AU").

Claim 1 is directed to a data transfer circuit for transferring a data group having data represented by plural bits from a first memory to a second memory for coding by a bit-plane coding processor. Detection means detects a maximum value in the data group as a transfer object, in which the detecting processing by the detection means is performed while transferring the data group and completed before completion of the transfer. Specifying means specifies a non-zero highest-order bit position among bits constructing the maximum value detected by the detection means, and outputs a code representing the bit position specified by the specifying means to the bit-plane coding processor. A bit in a position higher than the highest-order bit position specified by the specifying means is omitted from coding executed by the bit-plane coding processor after transferring the data group to the second memory.

Notably, in Claim 1, while transferring data, a maximum value in a data group as a transfer object is detected. Then a non-zero highest-order bit position among bits constructing the detected maximum value is specified, and a bit in a position higher

than the specified highest-order bit position is omitted from coding executed by the bit-plane coding processor. By virtue of the features of Claim 1, the number of bit-planes to be coded by the bit-plane coding processor can be reduced.

Yip EU relates to data compression, and in particular to an architecture for encoding coefficients that have been constructed as a result of a compression process. Fig. 3, cited in the Office Action, relates to a method of representing, or encoding, an image. The Office Action states, at page 4, that "Yip EU does not appear to disclose transferring 'from a first memory to a second memory for coding'". The Office Action also states, at page 4, that "Yip EU also does not disclose detecting 'while transferring the data group and completed before completion of the transfer'".

Yip AU relates to an encoding method and apparatus for representing a digital image. Fig. 6, cited in the Office Action, illustrates an encoder. In order to execute bit-plane coding, data transformation processing (606) and data analyzing (608-0...15) are executed for all bit-planes, upon data transferring from a memory (612 as shown in Fig. 6) to another memory (614,616, 618-0...15).

That is, in Yip AU, in order to execute bit-plane coding, data transformation processing (606) and data analyzing (608-0...15), the load of which are heavier than that of the processing for detecting the maximum value, must be executed for all bit-planes, and the number of bit-planes to be coded can not be reduced.

Even if, hypothetically, Yip EU were to be combined with Yip AU, such a combination would not attain the effects of Claim 1 in which the number of bit-planes to be coded can be reduced.

Nothing in Yip EU or Yip AU, whether considered either separately or in any permissible combination (if any) would teach or suggest (1) detecting a maximum value in a data group as a transfer object, wherein the detecting processing is performed while transferring the data group and completed before completion of the transfer, (2) specifying a non-zero highest-order bit position among bits constructing the detected maximum value, and (3) omitting a bit in a position higher than the specified highest-order bit position from coding executed by the bit-plane coding processor after transferring the data group to a second memory, as recited in Claim 1.

Accordingly, Claim 1 is believed to be patentable over Yip EU and Yip AU, whether considered either separately or in any permissible combination (if any).

Independent Claim 8 recites features which are similar in many relevant respects to those discussed above with respect to Claim 1 and therefore is also believed to be patentable over Yip EU and Yip AU for at least the reasons discussed above.

Claim 2 is directed to a data transfer circuit for transferring a data group having data represented by plural bits from a first memory to a second memory for coding by a bit-plane coding processor. Calculation means performs a logical OR calculation independently for each bit-plane, each bit-plane comprising bits which are located at the same bit position among bits constructing data which all the data group has. The processing of the logical OR calculation by the calculation means is performed while transferring the data group and completed before completion of the transfer. Specifying means specifies a non-zero highest-order bit position among bits constructing a result of the logical OR calculation by the calculation means, and outputs a code representing the bit

position specified by the specifying means to the bit-plane coding processor. A bit in a position higher than the highest-order bit position specified by the specifying means is omitted from coding executed by the bit-plane coding processor after transferring the data group to the second memory.

Notably, in Claim 2, upon data transferring, a logical OR calculation is performed independently for each bit-plane, each bit-plane consisting of bits which are located at the same bit position among bits constructing data which all the data group has. Then, a non-zero highest-order bit position is specified among bits constructing the result of the logical OR calculation, and a bit in a position higher than the specified highest-order bit position is omitted from coding executed by the bit-plane coding processor.

In Yip EU, a logical OR, for example B=B'+BitB1+BitB2+BitB3 is calculated. Each of BitB1, BitB2, and BitB3 indicates a logical OR calculation result of bits belonging to the current bit-plane. B' indicates the sum of the logical OR calculation results of each of higher-order bit-planes than the current bit-plane. However, for example, upon calculating BitB1 of the current bit-plane, bits used for calculating BitB1 must be searched among bits belonging to the current bit-plane.

However, according to Claim 2, since a logical OR calculation is executed independently for each bit-plane, this search processing is not necessary, and the encoding circuit can be made simpler than that of Yip EU.

Nothing in Yip EU or Yip AU, whether considered either separately or in any permissible combination (if any) would teach or suggest, upon data transferring, (1) performing a logical OR calculation independently for each bit-plane, each bit-plane

comprising bits which are located at the same bit position among bits constructing data which all the data group has, (2) specifying a non-zero highest-order bit position among bits constructing a result of the logical OR calculation, and (3) omitting a bit in a position higher than the specified highest-order bit position from coding executed by the bit-plane coding processor after transferring the data group to the second memory, as recited in Claim 2.

Accordingly, Claim 2 is believed to be patentable over Yip EU and Yip AU, whether considered either separately or in any permissible combination (if any).

Independent Claims 3, 4, and 9-11 recite features which are similar in many relevant respects to those discussed above with respect to Claim 1 and therefore are also believed to be patentable over Yip EU and Yip AU for at least the reasons discussed above.

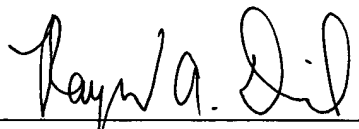
A review of the other art of record has failed to reveal anything which, in Applicant's opinion, would remedy the deficiencies of the art discussed above, as references against the independent claims herein. Those claims are therefore believed patentable over the art of record.

The other claims in this application are each dependent from one or another of the independent claims discussed above and are therefore believed patentable for the same reasons. Since each dependent claim is also deemed to define an additional aspect of the invention, however, the individual consideration or reconsideration, as the case may be, of the patentability of each on its own merits is respectfully requested.

In view of the foregoing amendments and remarks, Applicant respectfully requests favorable reconsideration and early passage to issue of the present application.

Applicant's undersigned attorney may be reached in our New York office by telephone at (212) 218-2100. All correspondence should continue to be directed to our below listed address.

Respectfully submitted,



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